Electrical Flight Control for Boeing YC-14

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By Martin Scott, Marconi Elliott Avionics YC-14 Programme Manager

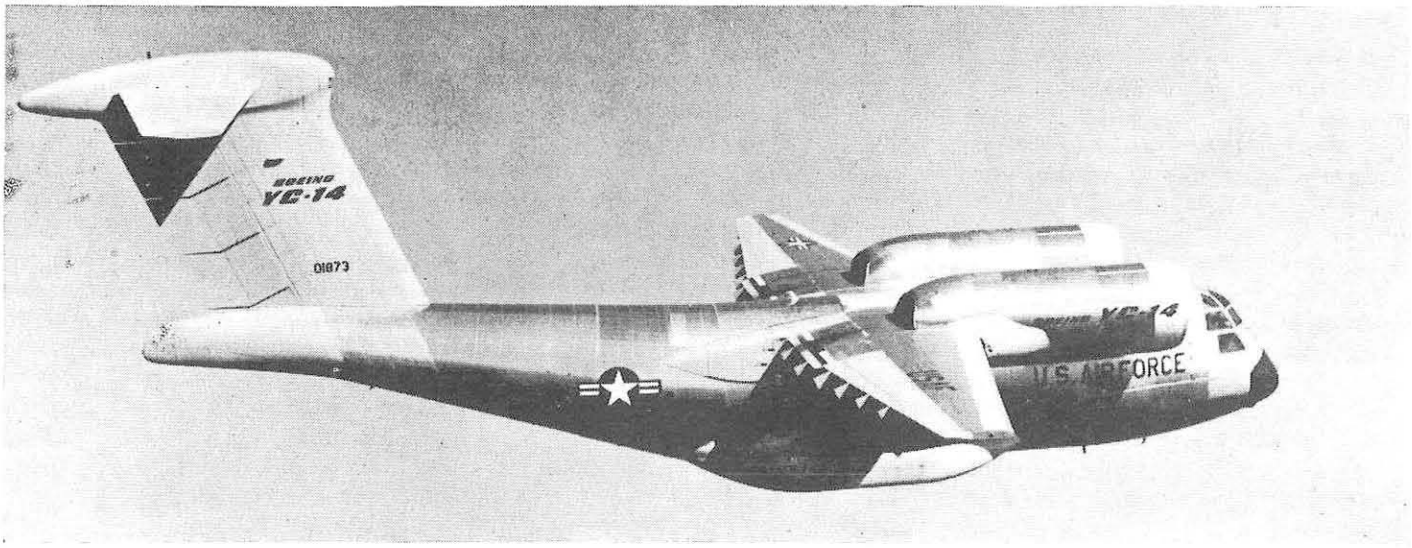


Figure 1

INTRODUCTION

The Boeing Company is manufacturing two prototype YC-14 aircraft as part of the United States Air Force Advanced Medium STOL (AMST) Programme. This programme is directed towards modern tactical airlift for the 1980's and the prototype aircraft are being built to demonstrate technology, performance and cost potential.

The requirements call for a high performance easy-to-fly aircraft manufactured to a design-to-cost goal of $5,000,000 (1972 dollars) production cost at the 300th unit. Towards achieving these goals, Boeing has employed unique design-to-cost manufacturing techniques in conjunction with a blend of proven off-the-shelf components and new control technologies. A large authority Electrical Flight Control System (EFCS) essentially provides fly-by-wire control of all primary aerodynamic control surfaces and engine thrust. This arrangement provides the excellent handling characteristics needed for safety and performance during STOL operation while reducing the crew workload to a level compatible with a two man flight crew.

The Flight Control Electronics (FCE), which is the heart of the triple redundant Electrical Flight Control Systems (EFCS) has been designed, developed and manufactured by Marconi-Elliott Avionic Systems Limited.

Their selection by Boeing for the YC-14 programme is a significant milestone for Marconi-Elliott Avionics in their development of high integrity digital flight control systems. This system, which embodies advanced technology such as optical data transmission, is the product of many years experience in the manufacture of high integrity automatic flight control systems and many other avionic systems.

THE BOEING YC-14 AMST

The Boeing YC-14 has been designed to meet the basic AMST "mission" performance requirement to carry 27,000 pounds (12,247 kg) of outsize payload 400 nm (740 km) to a 2000 ft (610 m) semi-prepared runway and return with a payload of the same weight without refuelling. Primary design flight conditions are:—

Short Take Off and Landing (STOL) characterised by 89 knots approach on a 6° glideslope. Operating lift coefficient (C_L) of $\geqslant 3.6$, which is over twice that of conventional transports.

High Mach number/high altitude cruise; entering regime of trans-

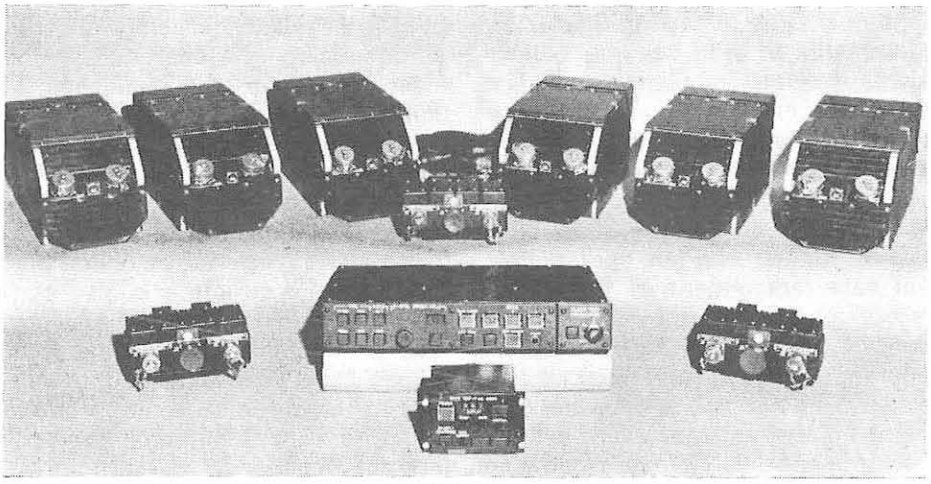


Figure 2

sonic aerodynamics.

Low altitude, high speed dash; imposing high dynamic pressures.

These flight conditions are illustrated in figure 3.

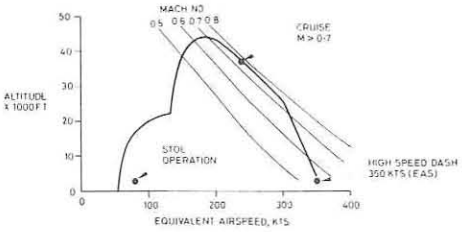


Figure 3

These requirements led Boeing to set the following design goals for the flight controls:

Excellent flying qualities using conventional piloting techniques—no special "STOL-mode" training.

Compensation for any powered-lift STOL characteristics; such as "back-side" of power curve effects.

Good engine-out performance.

Fail graceful characteristics (Gradual degradation of flying qualities with increasing number of failures).

The control surface configuration is shown in figure 4. The high lift system features the Upper Surface Blown (USB) flap arrangement in which the overwing mounted engines exhaust over the inboard trailing edge flap. This USB flap acts as a thrust vector control, rotating the thrust to nearly vertical on STOL landing approach. The USB flap is also used as a drag producing device in automatically holding the selected approach speed.

Increased lift is generated on the outboard wing by large circular-arc, double-slotted, trailing-edge flaps. Variable camber leading edge high lift flaps, of the same design as used on the Boeing 747, are used on the YC-14. Their useful operating angle of attack is further increased by Boundary Layer Control (BLC) blowing. Optimum performance is produced by scheduling the leading edge, outboard flaps and USB flaps separately.

The large, double hinged elevators and rudders produce about twice the control power of comparable conventional jet transports. Lateral control from ten spoilers and two ailerons is two-and-one-half times more powerful than for subsonic conventional take-off and landing transport aircraft. The control surfaces are commanded by large authority electrical signalling from the Electrical Flight Control System (EFCS). Full time mechanical signalling is also provided for all surfaces except the USB flaps, which are full fly-by-wire.

Functions provided by the EFCS

Command and stability augmentation:

Turn co-ordination, pitch and roll rate command, attitude hold and trim offload.

Speed and path control: throttle and USB flap speed control and direct lift control spoilers.

Configuration Management: fly-by-wire, USB flap, engine out sensing and flap compensation, air data sensor compensation, flight crew warning and air turbine driven hydraulic pump control.

Pilot assist modes: aerial delivery, pitch attitude trim and growth provisions for Altitude and Heading Hold and Flight Path Angle and Track Angle control modes.

The flight critical nature of the majority of these functions dictates a high integrity control system design for the EFCS. A fail operational/fail safe triplex configuration was required to meet the overall mission and safety reliability for the system. This concept extends from the sensors, through computing to the redundant split surface configuration. The redundancy level is reduced where appropriate for less critical functions.

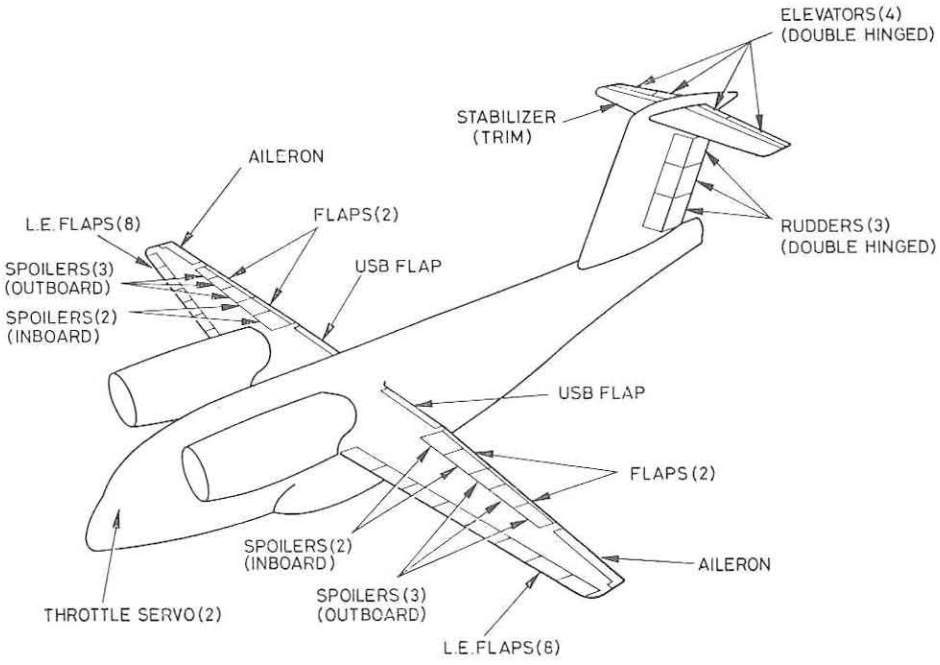


Figure 4

The Flight Control Electronics

(FCE) reflects this triplex fail operational system configuration and provides these functions:

Computation of control laws and mode logic.
Automatic detection and isolation of system failures.
Signal selection of all input signals.
Failure monitoring on all input signals and output commands.
Automated pre-flight system testing.
Modelling of functions not having segregated triplex actuation.

TECHNOLOGICAL BACKGROUND

The YC-14 EFCS is one of the most advanced production standard flight control systems yet produced. For Marconi-Elliott Avionics it represents the culmination of several years activity directed towards the integration of the company's well established backgrounds in Digital Avionic Systems and High Integrity Analogue Flight Control Systems. Although the movement towards digital mechanisations of many avionic systems was well under way in the late sixties, high integrity control systems posed the additional problem of needing to exploit the advantages of the digital mechanisation while maintaining the inherent safety or design background built up over the years on analogue equivalents.

Many of the analogue/digital trade-offs are similar to those in other applications and have been well aired elsewhere. While recognising the need for general purpose computers in certain applications, Marconi-Elliott Avionics have gone for "task orientation" in which the processor design is tailored towards the particular system requirement. Initially, this was directed towards hardware minimisation, but subsequently evolved towards improving interface design and optimising the performance of the total system. These processor developments were taking place in harmony with the development of other system elements, such as digital data transmission, displays, sensors etc. to provide a total digital system technology base. Of particular relevance to YC-14 was optical data transmission development. which had already produced flying systems capable of megabit transmission over tens of metres. As the particular requirements of high integrity control systems were considered against this technology background, systems could be designed without the constraints that stem from the need to use existing general purpose system elements.

The triplex, one-fail operational/fail safe requirement of the YC-14 is common to several current flight control applications. To be truly fail operational, the system must be free from common mode failures and dormant failures and not affect system performance during or following first failures. While many of the inherent analogue problems related to nuisance disconnect/failure transient/dormant failure trade-offs are minimised in a digital mechanisation, the extent to which the above aims can be achieved is still the essence of good system design. Common mode failure stems from four main causes:

External environment of the system
Inter-channel interference
Common design or manufacturing errors in the hardware
Common design or programming errors in the software (specific to digital systems)

In the essential similar redundancy design of the Flight Control Electronics, simplicity, visibility and rigorous testing and analysis are the main tenets for the avoidance of common design errors in both the hardware and software.

Relatively simple architectures were selected for the processing areas with a minimum of sophisticated and asynchronous operations. The software structure is also configured to aid testing and analysis. Normal modular programming techniques have been extended to provide a highly disciplined modular structure with minimum inter-modular communication and interaction. This approach, together with rigorous testing and analysis supported by computer aids for assembled programme analysis guards against programming and assembly errors as well as design errors. Hardware testing is similarly rigorous involving some 10,000 words of Acceptance Test Software specifically designed to exercise the hardware over the extremes of operation as well as considerable manual testing.

System reliability is assured through the use of established, in production, burnt-in components having good performance/reliability data bases, and is not predicated on small quantity, custom-made devices. A particular feature of the system is the use of inter-channel data

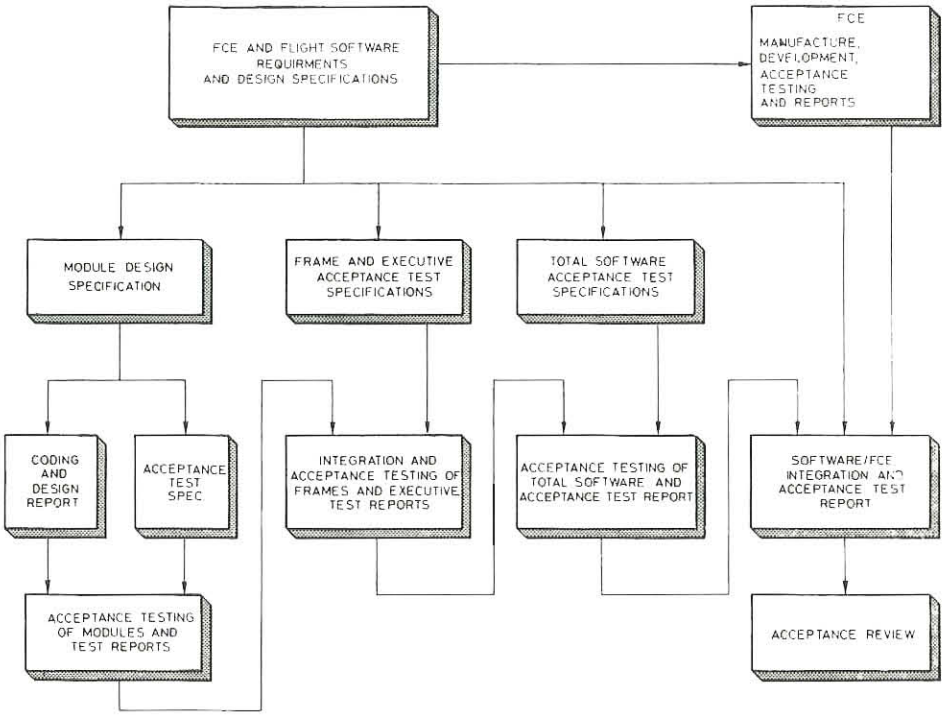
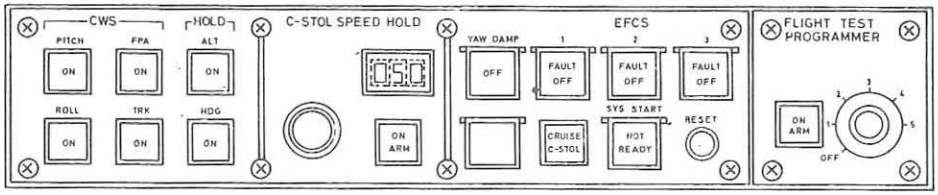


Figure 5

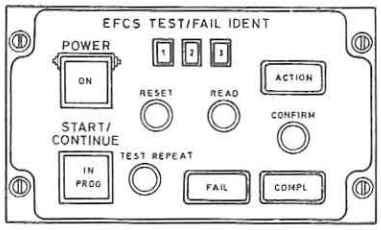
transmission via a single, time multiplexed optical highway. This eliminates the multiplicity of cross-channel analogue signal paths and associated circuitry that are an essential feature of multiple channel analogue systems. As well as the obvious advantages of electrical isolation, the use of fibre optics eliminates the risk of external sources of Electro Magnetic Inteference (EMI) corrupting these critical cross channel signals. Care is also exercised in the design of cross channel interfacing circuits and signal selectors and monitors to avoid inter-channel interference due to data corruption peculiar to a digital mechanisation.

The systems manufacturer can guard against common external sources of EMI, electrical power variation, etc., but the operation of the equipment with other aircraft equipment/systems must be established in conjunction with the airframe manufacturer.

An essential background to the successful development of the YC-14 Flight Control Electronics design has been the supply of sophisticated, failure survival flight control systems for such aircraft as the VC10 and Concorde, as well as the RAE Hunter Digital Autopilot and the fail safe digital Autopilot and Flight Director System (AFDS) on the MRCA.



CONTROL AND DISPLAY PANEL



TEST/FAILURE IDENTIFICATION PANEL

Figure 6

THE FLIGHT CONTROL ELECTRONICS (FCE)

Figure 5 shows a simplified schematic of the Flight Control Electronics (FCE). Signals from each of the triple redundant sources, such as rate gyros, accelerometers, air data systems and position transducers, pass directly to their corresponding Interface Units (IU). Here the signals are conditioned and converted from ac to dc and dc to digital as appropriate for onward transmission over a time multiplexed parallel digital highway to the associated Computer Unit (CU). A parallel to serial conversion takes place in the Computer Unit and the resulting serial data is transmitted to the Optical Coupler Unit (OCU). Here the electrical signals are converted into modulated light for transmission via the Optical Data Link (ODL) to the Optical Coupler Units in the other two redundant channels of the FCE.

The receiving Optical Coupler Units convert the received optical signals back to electrical signals for transmission to their associated Computer Unit. In this way, each Computer Unit receives the three signals from each sensor type; one directly via the Interface Unit and two indirectly via the Optical Data Links from the other two channels.

Signal selectors mechanised in the flight software select the "best" signal from each of the triple sensor values received. The signals are also monitored and any signal that exceeds a predetermined difference from the other two signals is automatically excluded and the source of the signal is declared as failed. The control laws, also mechanised in the software, are then computed using these "consolidated" signals as input data.

The computed output commands are transmitted from the Computer Unit back to the associated Interface via the time multiplexed parallel digital highway. Here they are converted back to analogue signals for summing with servo position signals to form servo commands. The Interface Unit also contains the drive electronics for all output servos.

Discrete input signals are converted to digital form in the Interface Unit, transmitted to the other channels and processed through signal selectors and control laws in a similar manner to the analogue sensor signals.

The operations of the processors in the three Computer Units are time synchronised via a fail operational software algorithm. This ensures that the three signals from each sensor type are processed simultaneously in the three Computer Units and that the same "best" signals are selected for the control law computations in the three channels. As the digital computations are identical in each channel, the tracking of the output commands is determined solely by tolerance control in the analogue output circuits in the Interface Units. Thus, once the inputs have been signal selected, the triple command paths do not require further consolidation but remain isolated through to the control surfaces.

System output failure monitoring is achieved by cross-comparison monitoring of the servo positions and modelled servo position if no actual servo exists for a given channel. Servo position signals are converted to digital form and transmitted across the channels in the same manner as sensor signals for this purpose. The cross-comparison monitors are mechanised in software, as is the failure logic, which establishes the need for isolation of functions or a complete channel.

Channel isolation signals are transmitted to separate hardware failure logic which is located in the Control and Display Panel (CDP). This triplicated logic performs majority selections of the "isolate" requests from each channel, and automatically isolates the requisite servos or other output devices for any failures occurring during C-STOL operation.

Failures occurring during cruise are presented to the flight crew as fault information allowing optional manual isolation. This difference in the approach to redundancy management is primarily due to the fewer active elements used during cruise and the less severe consequences of a failure during this part of the overall flight regime.

The flight crew manage the operation of the EFCS through the glare shield mounted Control and Display Panel shown in figure 6. From left to right across the front panel, CWS (Control Wheel Steering) is available with pitch attitude hold or flight path angle hold, and roll attitude hold or track hold. Conventional altitude and heading hold modes are also available as selectable modes. The C-STOL HOLD provides the capability to hold automatically the aircraft at a pre-selected speed during STOL operation.

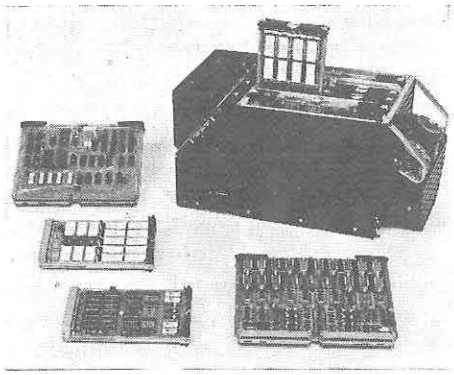


Figure 7

Configuration and redundancy management controls and displays are provided in the next part of the presentation. The three channel isolate switches provide manual isolation facilities together with displays of channel FAULT and OFF states. First failures may be reset by depression of the RESET switch, which resets the outputs from the failure monitors. The SYS START Switch is used to engage the EFCS following power up. NOT READY is displayed and system start is inhibited if the system is not in a valid state for flight. The CRUISE/C-STOL display indicates the system configuration for these flight regimes.

The FLIGHT TEST PROGRAMMER enables preprogrammed modifications to the control laws to be selected in flight. These modifications may be changed between flights by reprogramming the appropriate part(s) of the computer memories.

The TEST/FAILURE IDENTIFICATION PANEL, also shown in figure 6, is used to control the pre-flight testing to establish the flight readiness of the EFCS and for identifying failures in the system. In flight failures are also displayed as failure indentification numbers on this panel for diagnostic purposes and to aid the flight crew's management of the redundant configuration.

FLIGHT EQUIPMENT DETAILS

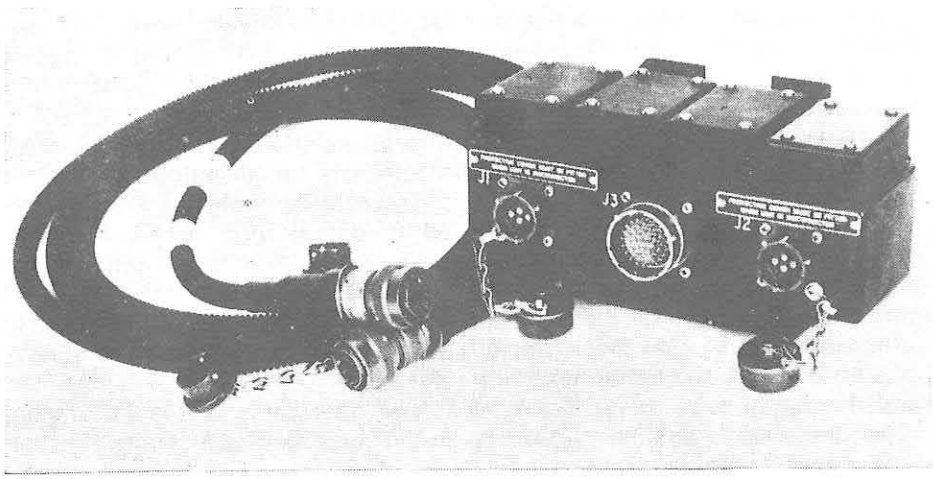
A full aircraft set of equipment comprises three Computer Units (CU), three Interface Units (IU), three Optical Coupler Units (OCU), three Optical Data Links (ODL), a Control and Display Panel (CDP) and a Test/Fail Ident Panel (T/FIP).

The Computer Unit (shown in figure 7) and the interface Unit are $\frac{3}{4}$ATR short LRU. Design, tooling and manufacturing costs have been minimised through the use of common chassis, card and PSU constructions for these two unit types. All of the processing, memory and digital interfacing circuits are housed in the Computer Unit. The 16 bit processor includes features specific to fail operational applications and operates in conjunction with semi-conductor memories providing a total memory capacity in excess of 16,000 words. A parallel digital highway provides communication between the Computer Unit and the Interface Unit. Analogue and discrete conditioning circuits contained in the latter unit reflect the particular interfacing characteristics of the YC-14 EFCS and include autothrottle and electrical command servo amplifiers and flight test interfacing circuitry.

The Optical Coupler Unit, shown in figure 8, contains the electrical/optical and optical/electrical interfacing circuits for the cross channel serial digital signals. While Marconi-Elliott Avionics had developed fibre optic components for other optical data transmission systems, which had been subjected to extensive flight testing by the Royal Aircraft Establishment (RAE), and had the manufacturing capability for YC-14, Bowthorpe Hellerman were selected to supply the fibre optic components, because of their previous work in optical and electrical connectors. Their Electronic Components Division has supplied the Optical Data Links (ODL) and optical sub-assemblies for fitting in the Optical Coupler Unit to a Marconi-Elliott specification. Environment and handling tests conducted by Marconi-Elliott Avionics and Boeing have shown this optical data transmission to be as rugged an any electrical equivalent.

As much a computer as a panel, the Control and Display Panel (CDP) contains three channels of failure logic as well as switches and displays. Triple, segregated contact switches are employed except for the channel isolate switches, which are simplex one/channel. The indicators are dual redundant, being driven from pairs of channels. Discrete signals are transmitted between the redundant channels via optical isolators. Figure 9 shows this panel with cover and some partitioning removed.

Figure 8



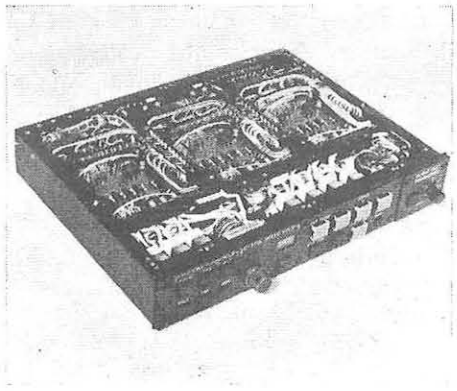


Figure 9

FLIGHT SOFTWARE

In this flight critical application, good management and control of the in-flight software development is essential to ensure a high level of system integrity. Software design or programming errors can constitute common mode failures of the system and the probablity of a single software error occurring must be very remote.

The software is structured in a modular manner consistent with good programming practice. The module size is determined by the need to assimilate and understand them as entities, the amount of their input/output data and the number of decision points they contain. Module boundaries, entry and exit procedures, and intermodule communications are strictly defined. The use of processing facilities available in the computer are strictly controlled, specifically excluding sophisticated facilities that can introduce complexity into the software. The intent of these rules is to produce modules that can be thoroughly tested as separate entities, and when integrated, have the minimum amount of interaction. This enables the integrated modules to be tested without reference to their internal structure. For example, a 10,000 word programme may be structured as 10 segments, each containing 20 modules of 50 words. The scope of testing at each level is comparable, because, as the amount of data flow between the entities increases with the level of integration, the number of entities being tested decreases.

The overall software development process begins with the Requirements and Design Specifications for the Flight Control Electronics (FCE) and the flight software as shown in figure 10. Module Design Specifications are then drawn up and testing continues in a rigorous, formally controlled manner, with particular attention being paid to the adherence of the modules to the programming rules. Testing at module level is primarily concerned with proof of compliance of the programmed code with the appropriate Module Design Specification. These modules are integrated into frames, which are related to the timing structure of the software. Frame level testing is concerned with proof of compliance of the Software Design Requirements. The frames are then fully integrated and tested as a complete programme, again for compliance with the Software Design Requirements. Finally, the flight software and the Flight Control Electronics are subjected to an integration test to prove compatibility between the hardware and software designs.

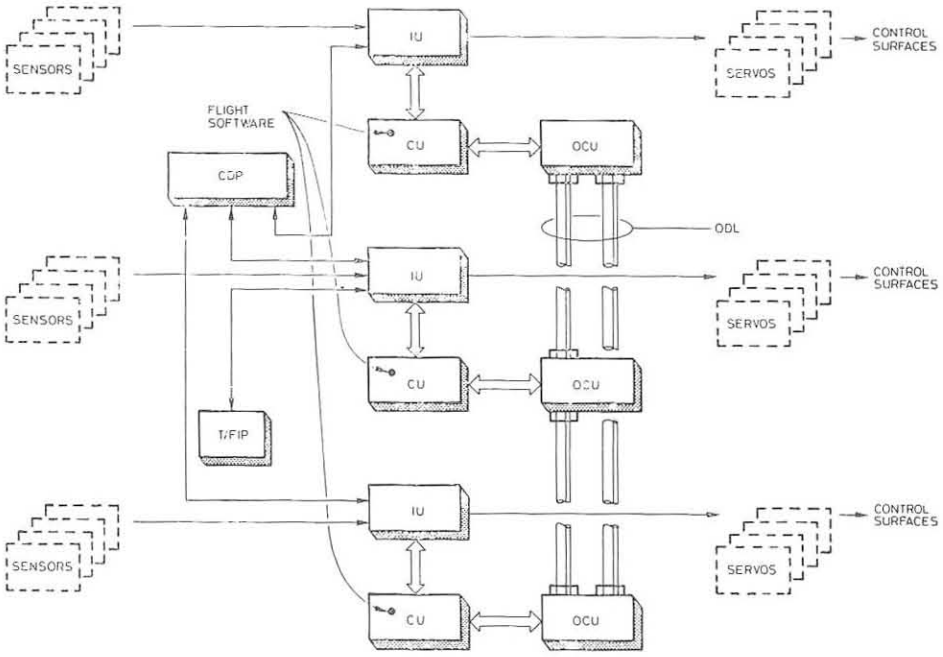
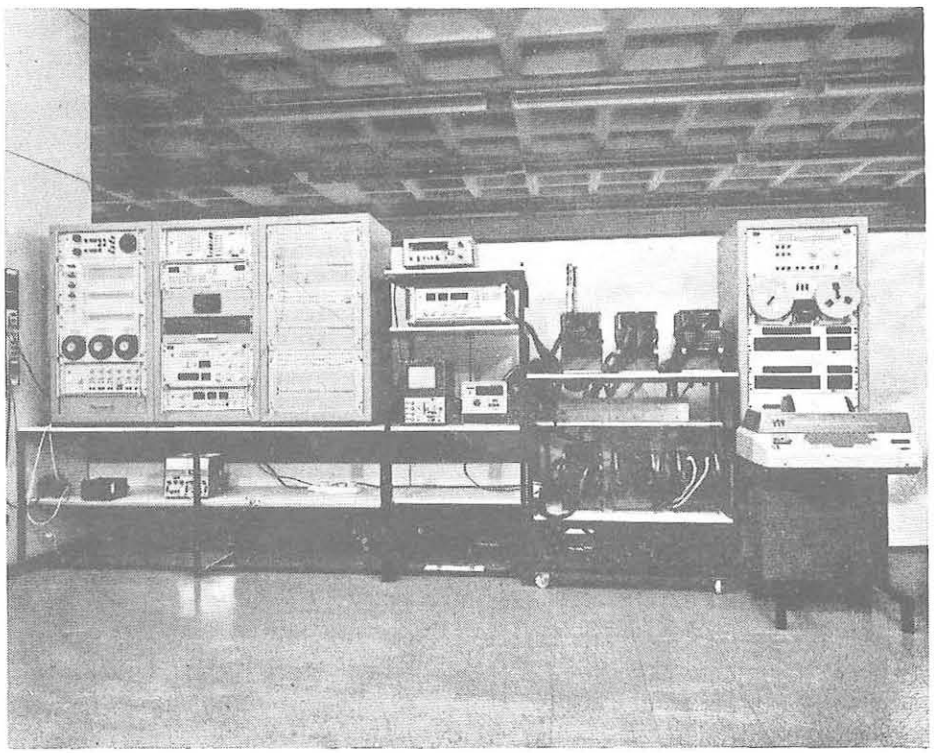


Figure 10

While all of this testing ensures

Figure 11



initial compliance with the Design Specifications and Requirements it must be viewed in the context of the overall testing programme, involving closed loop testing with simulations of aircraft dynamics, with EFCS interfaces, through to flight testing of the aircraft. The entire software development process is thoroughly documented and subjected to as strict configuration and quality control as the hardware. These procedures will also be adhered to by Boeing throughout the YC-14 Programme.

The FCE is tested at three levels; unit, channel and full triplex system. Much of this testing is automated through the use of Acceptance Test Software (ATS) written specifically to exercise the hardware. Running to over 10,000 words programmed into each Computer Unit, this software provides functional testing at all three levels and comprises an extensive software library which is not necessarily related to the flight software. These automatic tests are augmented by manual testing in conjunction with the Acceptance Test Software in those interface areas not amenable to automatic testing and for certain timing tests.

Testing at full triplex system level centres on the operation of time synchronisation cross channel data transfer, panels interfaces and failure logic. Figure 11, shows the Ground Support Equipment (GSE) set up for system level testing during the system development phase. This test equipment is designed to be used for maintenance at unit level and for flight software development at system level. The test equipment is compatible with the interfacing of a hybrid digital/analogue computer to the flight equipment for this latter purpose. Prior to delivery, it is used for unit and system development and acceptance testing at unit, channel and full triplex system level.

A core memory unit, also shown in Figure 11, is supplied with the flight equipment to aid software development in the laboratory. When interfaced to the Computer units, this unit takes over from the computer's internal non-volatile reprogrammable memories enabling on line corrections to be made to the software during development.

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