The Design and Development of the MRCA Autopilot

Presented to
AGARD 17th GUIDANCE and CONTROL PANEL SYMPOSIUM

Advances in Control Systems

24th – 26th September 1973 at Geilo Norway
THE DESIGN AND DEVELOPMENT OF
THE MRCA AUTOPILOT

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SUMMARY

The design and development of the MRCA Autopilot and Flight Director System (AFDS) is described. Particular reference is made to the problem of ensuring flight safety in the low altitude autopilot modes. Included are discussions of design philosophy, system configuration and control tasks, together with hardware and software implementation.

The work described is being carried out by a team comprising Marconi-Elliott Avionics (England) and Aeritalia CEA (Italy) personnel; the companies are sharing both the development and manufacturing work on this project.

Introduction

The MRCA Autopilot and Flight Director System (AFDS) is designed to provide automatic control of the aircraft in the pitch and lateral planes in a variety of operating modes. A flight director facility is included which provides signals to the pilot's instruments to enable the pilot to monitor the autopilot performance and to use for flight path guidance if an autopilot malfunction occurs.

Included in the autopilot facilities are an autothrottle which provides airspeed hold by means of thrust control, and pitch auto-trim which continuously controls the pilot's stick to the pitch trim position.

The principal means by which the autopilot controls the aircraft is by providing manoeuvre demand signals to the Command Stability Augmentation System (CSAS). This is a triple redundant, fly-by-wire primary flight control system and the interface between the Autopilot and the CSAS is an important feature of the design. A simplified schematic of the system is shown in figure 1.

Figure 1 AFDS configuration

The following modes of operation are provided:
- Terrain Following (or Radar Height Hold)
- Barometric Altitude Hold
- Pitch Attitude Hold
- Heading Hold
- Heading Acquire
- Mach Number Hold
- Auto Approach (ILS or SETAC)
- Track Acquire
- Bank Attitude Hold
- Calibrated Airspeed Hold (Auto-throttle only)
The configuration of the AFDS has been largely constrained by the following requirements:

(a) It must be capable of providing safe automatic control of the aircraft especially in the low altitude modes.

(b) The flight director facility should in general remain available after a single failure in the AFDS or its output to the CSAS has caused autopilot control to be disconnected.

The initial requirement essentially implies a 100% failure detection probability. Although this figure could possibly be approached in a simplex self monitored digital processor with an all digital interface, difficulties arise in the area of the analog interfaces in particular with the CSAS. Therefore it was decided that similar redundant duplex lanes would be necessary for the autopilot computing.

The requirement for a fail survival flight director facility meant either that a further computing lane dedicated to flight director be provided or, given a high self monitoring capability in the duplex autopilot computing lanes, a failure of one lane can result in the automatic selection of the good autopilot lane for the reversionary flight director facility. Figure 2 shows this alternative in diagrammatic form. By implementing this arrangement with self monitored digital processors, a minimum hardware solution has been achieved and this has been finally selected as the system to be developed.

Figure 2 Duplex autopilot with reversionary flight director.

In addition to the above-mentioned self monitoring capability which could be built into the digital processors, the digital solution offered various other advantages compared with an analog solution, in particular it has given a flexibility in control law design; ie the possibility of a large degree of independence of hardware development and system development; this has proved particularly beneficial due to the tight time-scales of the project. Also, improved computational accuracy, has been achieved especially when the complete temperature range airborne environment is considered.

System Development - Output Redundancy and Cross-monitoring Arrangements.

Having decided upon the use of dual redundant digital processors for the autopilot computing, the next question was - how to consolidate the pitch and roll rate demand outputs to the CSAS and how to provide acceptable flight director, autothrottle and autorim outputs.

As regards the pitch and roll rate outputs, these signals are necessarily triplex analog in nature so as to be compatible with the CSAS computing and as the arguments in favour of dual redundancy for the digital processors apply equally to the digital to analog conversion, it was decided that each computer should provide analog outputs which could then be consolidated by analog crossfeeds to the other

computer, and that AFDS Computer 1 should include the necessary triplex hardware to consolidate the signals to the CSAS. Figure 3 shows this output consolidation for the pitch channel; the roll channel is identical except that triplex averagers are used in place of the more nose up units.

![Figure 3 Consolidation of triplex pitch demand outputs](image)

In the pitch channel the analog outputs from each AFDS Computer are taken to 'more nose up' (MNU) circuits in order that the demand signal to the CSAS will always be the more positive of the two computer outputs. This technique is used to effectively eliminate the possible aircraft nose down excursion due to failure in one of the computers, allowing fairly long comparison monitor time delays to be implemented so as to minimise nuisance disconnect problems. In the roll channel the analog outputs from each AFDS Computer are averaged before being taken to the CSAS. This reduces the disengagement transient by a factor of two compared with the alternative simplex monitored configuration.

The flight director output to the HUD has been specified as a simplex serial digital transmission channel. Each AFDS Computer contains the necessary digital serialiser hardware to be capable of providing the interface to the HUD itself. In the absence of faults the output to the HUD is taken from Computer 2. Should a fault be detected, and located to this computer, then the digital output from Computer 1 is automatically selected to enable flight director capability to be maintained. The digital output to the HUD is also paralleled by dc analog outputs to the cross pointers of the attitude director indicator.

The autothrottle system is essentially duplex, except that a single monitored actuator is used to drive the pilot's throttle levers; its essential features are shown in figure 4.

![Figure 4 Autothrottle system](image)
An important feature of the configuration is that the stick feedback loop not only keeps the autopilot number of benefits which include the capability of rapid stick trimming after a turn entry, and during with the result that it can be much faster in operation than, for example, a configuration which keeps the autopilot output nulled by means of the auto-trim / CSAS / aircraft loop. This arrangement has quite a output via the stick feedback loop. malfunctions, and inadvertent stick application in the low level modes can be cancelled. figure 5 shows the drive and monitoring scheme adopted.

A pitch stick position feedback loop is used to enable the transfer of the total autopilot demand signal (point A in figure 5) to the CSAS (point B). It will be seen that this signal transfer consists of a steady state component provided by the control stick pick-off via the auto-trim loop, plus the variations about the steady state provided by the direct electrical output to the CSAS. When this output to the CSAS exceeds the trim drive non-linearity threshold, the auto-trim operates in such a direction as to null the autopilot output via the stick feedback loop.

An important feature of the configuration is that the stick feedback loop not only keeps the autopilot output nulled but also does not cause any net input to the CSAS during the trimming process. Therefore the speed of the auto-trim is determined only by the stability of the auto-trim drive/stick feedback loop with the result that it can be much faster in operation than, for example, a configuration which keeps the autopilot output nulled by means of the auto-trim/CSAS/aircraft loop. This arrangement has quite a number of benefits which include the capability of rapid stick trimming after a turn entry, and during manoeuvres such as terrain following; there is also no effect on aircraft flight path due to auto-trim malfunctions, and inadvertent stick application in the low level modes can be cancelled.

Pitch auto-trim is operated in all pitch modes of the autopilot, a drive signal generated in Computer 2 controlling the auto-trim motor so as to maintain the control stick in the trimmed position. Incorrect operation is detected by means of monitoring logic included in the computers. Figure 5 shows the drive and monitoring scheme adopted.

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The following is a list of these AFDS monitored inputs.

<table>
<thead>
<tr>
<th>Input Parameter</th>
<th>Form of Monitoring</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch Rate</td>
<td>Duplex</td>
<td>Redundant sources with low authority synchronisation within CSAS.</td>
</tr>
<tr>
<td>Yaw Rate</td>
<td>Simplex</td>
<td>Inertial platform data monitored by standby attitude reference data.</td>
</tr>
<tr>
<td>Roll Rate</td>
<td>Simplex</td>
<td>Consolidated within CSAS.</td>
</tr>
<tr>
<td>Bank Attitude</td>
<td>Simplex</td>
<td>Air data system monitored by derived data from triple transponder unit.</td>
</tr>
<tr>
<td>Pitch Attitude</td>
<td>Simplex</td>
<td>Air data system monitored by derived data from triple transponder unit.</td>
</tr>
<tr>
<td>Dynamic Pressure</td>
<td>Simplex</td>
<td>Air data system monitored by derived data from triple transponder unit.</td>
</tr>
<tr>
<td>True Air Speed</td>
<td>Simplex</td>
<td>Air data system monitored by derived data from triple transponder unit.</td>
</tr>
<tr>
<td>Wing Sweep</td>
<td>Simplex</td>
<td>Air data system monitored by derived data from triple transponder unit.</td>
</tr>
</tbody>
</table>

System Development-Control Laws.

The control laws defining the system operation of the autopilot and flight director are in general implemented digitally, using the identical processors contained in Computers 1 and 2, although certain functions, which require a degree of fail survivability, are implemented with triplex analog hardware. These relate to the interface with the CSAS and are associated particularly with the autopilot disengagement function.

It is convenient to consider these control laws in terms of blocks which are split into functional sections. These functional sections are, in fact, closely related to the computing blocks included in the time-shared processor programme cycles, which perform repeat computations of the selected control laws at a fixed iteration rate of about 30 per second. These sections, and their inter-relationship, are shown in figure 6.

Figure 5 Auto-trim

Input Signal Redundancy

The input signals to the AFDS fall into three groups. Firstly, signals associated with non-critical modes, such as barometric height hold, are not redundant or fully monitored and failure protection is provided by maneuvre limits included in the two computers. The second group comprises those signals which are fully monitored at source, two correct signals being sent to the AFDS; examples of this type of signal are radar height signal for radar height hold mode and vertical acceleration command for terrain following. Finally there are a number of inputs where signals from various sources are used and the monitoring is performed in the AFDS.

The interface between the pitch channel mode computing and output section is always characterised by a vertical acceleration demand signal, and the interface between the roll channel mode computing and output section is always characterised by a bank angle demand signal. The following is a brief discussion of the significant features of the various control laws at their current state of development.

Figure 6 AFDS computing blocks.
The pitch axis output section is shown in figure 7. This computing section includes the processing of the incremental vertical acceleration demand input signal into a suitable form for the pitch channel of the CSAS (autopilot mode), for the HUD and ADI displays (flight director steering and monitoring) and for the pitch auto-trim.

The pitch axis output section has been designed to meet the requirements of that particular mode to be satisfied. The features of the various pitch axis modes are discussed briefly below.

It will be noted that the incremental vertical acceleration demand signal which is derived in the mode computing section is resolved into (absolute) normal acceleration demand. An upper normal acceleration limit is introduced to keep the demanded normal acceleration with safe limits. In order to improve the overall matching between the two computing lane, a small authority cross-feed synchronisation term has been introduced part way along the computing chain, at A'. The auxiliary pitch rate loop with proportional plus integral control of pitch rate error has been recently introduced in order to effectively eliminate the variation of steady state closed loop gain of autopilot/CAS combination. This has proved necessary because of the difficulties experienced in trying to establish a CSAS pitch rate loop which would meet both the short period damping and handling qualities for manual flight, and the necessary performance for the autopilot.

The flight director pitch axis control laws are divided into acquire modes (terrain following, auto-approach), and hold modes (all other modes). In the acquire modes, a high bandwidth control law is used, based on pitch rate error and this is scheduled with true airspeed in order to nominally represent normal acceleration error. The control laws for the flight director pitch axis hold modes are based on the provisions of a vertical acceleration demand display deflection to the HUD and ADI. As this vertical acceleration demand signal is in turn derived from the outer loop error, these outer loop errors will be eliminated as the pilot keeps the display deflection nulled.

Preliminary "man in the loop" fixed base simulations have indicated that acceptable control will be achieved with these display deflection algorithms.

The function of the mode computing section is, on receipt of mode select instructions, to provide to the pitch channel output section the appropriate vertical acceleration demand signal to enable the performance requirement of that particular mode to be satisfied. The features of the various pitch axis modes are discussed briefly below.

The roll axis output section is shown in figure 8.

Amplitude limits on the input bank angle demand are included in order to implement a pitch axis priority by reducing the bank angle for large pitch axis demands to limit the turn rate. The cross-feed consolidation B', which is a low authority averaging synchroniser, has been introduced to improve the overall lane matching. Roll rate limits, which depend on mode selected, are included in order to give the required performance in both autopilot and flight director. A "stick cancel" loop, required to...
Computer 2. The digital processors in AFDS Computers 1 and 2 are identical to each other in all aspects, as are the analog and digital input and output interfaces to the processors. The differences are confined to the heading hold circuitry and the interface to the aircraft's navigation system. The control law for the heading hold station is such that the demanded bank angle depends on both the across-track displacement and the Instantaneous velocity vector to the position of the aircraft.

In order to keep the hardware content to the minimum, 12 bit parallel operation has been adopted, and as a result, 12 bit parallel read/write interface is used. The function is normally implemented either by a polynomial series, a segmented straight line approximation of the function, or an arithmetic operation (say multiply, add) depending on the form of the function being used. The high accuracy of the digital processors, it is necessary to take particular care in scaling the various parameters, and in certain cases double length working has been used so as to eliminate the possibility of accumulator overflow while retaining the necessary response for good low amplitude system performance. For example, in the evaluation of control filters, it is necessary to use double length storage of integrator states and double length working for integrator update.

The computation accuracy available with a 12 bit machine (of the order of 0.05%) is better than that achievable with an analog machine, especially when one considers multiplication, division, and non-linear function generation.

Function generation in the AFDS is normally carried out as combinations of functions of single variables.

\[ f_1(x) = a_1 x + b_1 \]

where \( f_1 \), \( f_2 \), \( f_3 \) are normally implemented either by a polynomial series, a segmented straight line approximation of the function, or an arithmetic operation (say multiply, add) depending on the form of the function and its accuracy requirements. Trigonometrical functions are generally implemented by polynomial series.

Despite the high accuracy of the digital processors, it is necessary to cross synchronise the output of those computing lanes which include integral control such as the pitch channel autopilot, and auto-throttle. Since the digital inputs are used in the integral control, the integral control could result in an output which is different from the analog control. The effect of using asynchronous processors in time dependent functions such as control filters and datum adjust inputs.

The processor performs all data input and output processing, program decoding, storing, and arithmetic functions. These operations are carried out under the control of the 32 ms program cycle clock. An autonomous data transfer facility provides external access to the processor data store via an extension to the data store bus. The processor controls access to the data store via an access control logic. This is because the processor can operate simultaneously with an autonomous data transfer unit, hence the requires access to the data store.

The work done to date confirms that the program iteration rate of about 30 cycles per second will give adequate performance for the control law being used. Tests have included the use of the company's hybrid computer facility which has been programmed so that the analog part represents the aircraft and its flight control system, while the digital part represents the autopilot/flight director. In order to do this, it has been necessary to appropriately program the digital computer to provide 12 bit operation with the same scaling factors as the AFDS computing. The level low level assembler language of the AFDS is closely matched by the assembler language available on the hybrid machine, hence the effects of resolution, rounding, errors, sampling and time delays have been able to be investigated. The update period of 32 ms has been simply achieved by utilizing the interrupt facility of the computer.

The processor instruction code has been chosen to require minimum hardware consistent with program length. Fourteen instructions are used, and this number has been found to be quite adequate, as only about 30% of the available processor cycle time is currently being employed.

The computer program includes sections for control laws, mode logic, and BITE. Out of the 4096 words of program store, approximately 1200 are used for control laws, 1300 for model logic and 1000 for BIT. The computer stores approximate 600 word storage capacity. The BITE function, which is of particular importance in detecting a failed lane and hence providing a failure survival flight director, consists of on-line (continuous interleaved) and off-line (manual not engaged) checks.

The on-line check involves an instruction sequence to produce a unique number by exercising all of the functions of the processor arithmetic unit. An analog interface check is also included; this involves an output to input digital-analog, analog-digital loop check. Also, the scratchpad stores parity bit locations in order to immediately detect any corruption of data.

The off-line check which are immediately initiated when the autopilot disconnects due to computer failures include, in addition to the above on-line checks, a software controlled check of analog and digital interfaces and discrete input buffers. The analog loop check includes all 13 analog inputs; the digital loop check includes all words of all 3 digital data input channels, including checks of parity, control, and spare bits. It is expected that these off-line processor interface checks will enable the reversionary flight director facility to be achieved with at least 95% confidence. Comprehensive tests are also carried out in the manually initiated pre-flight and first-line tests.

System Hardware

The AFDS comprises the following units:

- **AFDS Computer 1**
  - Roll Force Sensor
  - Pilots Control Panel
  - Autopilot Actuator

- **AFDS Computer 2**
  - Pitch Force Sensor
Figure 10 Typical logic and store cards

Each computer is housed in an ARINC standard ATR short box, and includes power supplies at the rear and twenty electronic cards.

Figure 11 shows one of the computer boxes. Approximate weight of the computers is 29 lb. each.

The system electronics, including power supplies and input/output interfaces, are housed in the two computers. The two processors, one in each computer box, are identical, but there are minor differences between the two computers in that Computer 1 contains the consolidated tripex outputs to the CSAS, and Computer 2 contains the servo drives for both the autothrottle actuator and the pitch auto-trim actuator.

The processor logic is based on TTL-type components which are mounted on double sided printed circuit boards. The store components will be bipolar type ROMs in the production equipment but in order to provide the capability for rapid change during flight test, erasable PROMs will be used in the development equipments. Typical interface and store cards are shown in Figure 10.

Figure 11 Autopilot/flight director computer

The Pitch and Roll Stick Force Sensors (figure 12) are mechanical spring-switch mechanisms which are installed in the control runs and which detect fixed force levels for the automatic steering override facility and for emergency stick force cut-out required in the low level autopilot modes.

Figure 12 Force sensor unit

The pilot’s control panel shown in Figure 13 includes momentary contact push button switches for selecting the various modes of operation, a terrain following clearance height selector and ride control, and datum adjust switches for barometric altitude hold, Mach number hold, and autothrottle. A spring loaded flap covers the pre-flight and first line test controls.

Figure 13 Pilot’s control panel

Figure 14 Autothrottle actuator

Concluding Remarks

The major features of the MRCA Autopilot and Flight Director System have been described. The project is now well advanced and hardware is being delivered to the airframe manufacturers. Considering the complexity of the system, the development programme has gone well, and there is no doubt that the digital nature of the system has contributed significantly to this situation.

The flexibility, accuracy and self test capability of the digital processor are major advantages which can now be obtained economically and it is clear that except for the simplest applications, all future automatic flight control systems will be digital.